

SiNFP-32xx Flow Processor:

Ruggedized Netronome NFP; 133 MHz DDR3

Preliminary Product Feature Sheet

Product Highlights

- Source-code compatibility (including backwards-compatibility) with Intel® IXP28XX microengines for customer application migration
- High-performance solution with low power consumption for a broad range of L2-L7 applications, delivering up to 30 Mpps/20 Gbps packet forwarding, policing, scheduling, queue management and protocol interworking, and 70-million enqueue/dequeue packet operations per second, enabling deep packet processing of 64-byte Ethernet packets with no loss of performance
- Enhanced microengine (v2.7) derived from the latest Intel version (v2.6); 40 separate microengines with eight threads each running up to 1.6 GHz
- High-performance 32-bit ARM11, plus L2 cache, for processing complex algorithms, route table maintenance, control plane, and system-level management functions
- Two DDR3 DRAM interfaces support more than 70 Gbps of total bandwidth
- High-performance SRAM supports more than 300 MQOps (queuing operations/second)
- High-speed PCIe 2.0 interface to multicore x86 or external control plane processor
- Standards-based interfaces for easy integration (e.g., QDR II, DDR3, PCIe 2.0, XAUI, Interlaken)
- Packet and content processing with robust security features in a single component reduces system cost by eliminating need for multiple devices.
- Integrated cryptography engines provide hardware acceleration of multiple algorithms (including all currently standardized AES variants) performing IPSec encryption/decryption at up to 20 Gbps
- Fully programmable network processor architecture enables optimization of additional algorithms and protocols to support IPSec, TCP and SSL application environments

Device Overview

For designers of communications equipment whose network processing requirements extend beyond simple forwarding, Netronome's Flow Processors deliver high-performance packet processing with intelligence, security and virtualization for millions of simultaneous flows.



Unlike network processors and multicore CPUs that lack L4-L7 programmability or cannot scale to 10 Gbps and beyond, Netronome's flow processors are powered by 40 programmable networking cores that deliver 2,000 instructions and 50 flow operations per packet at 30 million pps, enabling 20 Gbps of L2-L7 processing with line-rate security and I/O virtualization.

Specifications:

Microengine v2.7 (8k instructions or 16k shared between 2 MEs; 1k-word local memory): 32-bit data path; up to 40 MEs and 320 threads; 56 billion instructions per second; 1,800 instructions per packet and 1.84 billion instructions per watt	
Operating Temperature	-55 °C to 125 °C
Power Dissipation	~20 W minimum
Solder Ball Pitch	1 mm
SPI-4 Phase 2 Operation	250-500 MHz (622-1,000 MTs) 16-bit LVDS (dual-edge) signaling
XAUI Interface	3.125 GHz for 4 lanes supporting 10 Gbps operation
Interlaken Interface	6.25 GHz per lane (each of the 4 lanes supports 3.125-6.375 GHz operation)
ARM11 Core Operating Frequency	700 MHz, 500 MHz and 325 MHz/32-bit data path
GEN-II PCIe Interface	Version 2, x8 (5.0 Gbps/lane, 40 Gbps total each way)
SRAM Interface (QDR)(two channels)	Peak bandwidth of 2 GBps channel using 250 MHz SRAMs (1 GB Read, 1GB Write)
DDR3 DRAM (two channels)	Peak bandwidth 8.5 GBps (68.2 Gbps) for 64-bit channel

Packaging

- 1521 Ball FCBGA 40 mm x 40 mm ROHS Compliant Package

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Power Supply Voltages:

ME V _{dd} Voltage	1.125 V ± 3%
ARM11 Core V _{dd} Voltage	1.5 V ± 3%
Memory I/O Voltage	1.5 V ± 5%
GEN-II PCIe I/O Voltage	1.0 V ± 3%
SPI4.2 I/O Voltage	2.5 V ± 5%
Interlaken Voltage	1.0 V ± 3%

Netronome Network Flow Engine Family

Features	Benefits
40 microengines, each with eight threads and 8k-words of control store	High-performance, flexible, multi-threaded, RISC processor engines that are easily programmed for a variety of packet processing applications. Paired microengines provide 16k word shared instruction stores for run-to-completion or pool-of-threads programming model
Integrated ARM11, L1 cache (32 KB instruction cache, 32 KB data cache) plus L2 cache (256 KB)	Embedded 32-bit RISC core for IKE, route table maintenance and system-level management function help to lower system cost and save board space
Integrated PKI and cryptography blocks provide hardware acceleration for DES, 3DES, AES, SHA-1 and SHA-2 algorithms	Enables bulk encryption/decryption for IPSec data streams at speeds up to 10 Gpbs
Flow-through cryptography architecture processes packets “on-the-fly”	Increases performance and helps to minimize packet reassembly in memory
Two programmable, unidirectional 16-bit LVDS data interfaces. One interface can be a single, bi-directional SPI-4 Phase 2, 1x10GbE MAC, 4x1GbE MAC or Interlaken interface. The other can be a single 1x10GbE MAC, 4x1GbE MAC or Interlaken interface	Supports industry-standard interfaces to media and fabric devices, delivering greater than 10 Gbps performance rate. Standard interface to I/O appliances, MACs/framers, and fabric interface chips. Standard interface supported by FPGA and ASIC vendors.
Two industry-standard DDR3 DRAM interfaces (two 64-bit)	High-density, high-bandwidth memory subsystem. Supports up to 8 GB of system DRAM memory.
DRAM-optimized cache	2 MB of internal cache, optimized to maximize the DDR performance and provide two additional “virtual QDR” channels
Two industry-standard 32-bit QDR SRAM interfaces	Multiple-channel, fast access to lookup tables, access lists, statistics and data structure control. Supports industry-standard NPF LA-1 interface for TCAM or look-aside processor additions
PCIe 2.0 x8 I/O interface	Supports industry-standard connection to x86 or other control plane processors with PCIe 2.0 widths of up to eight lanes
Hardware support for memory access queuing	Simplifies memory queue structures and software support by utilizing internal hardware acceleration
JTAG Support	Standard board-level debug support
Software Development Kit and Hardware Development Kit	Shortens user development time

Product Availability

Netronome delivers a family of BFP-3200 Flow Processors to the market addressing various feature and performance points - from the NFP-3216 (16 MEs) to the NFP-3240 (40MEs) - with all of them available in a RoHS-compliant 1521 FCBGA package.

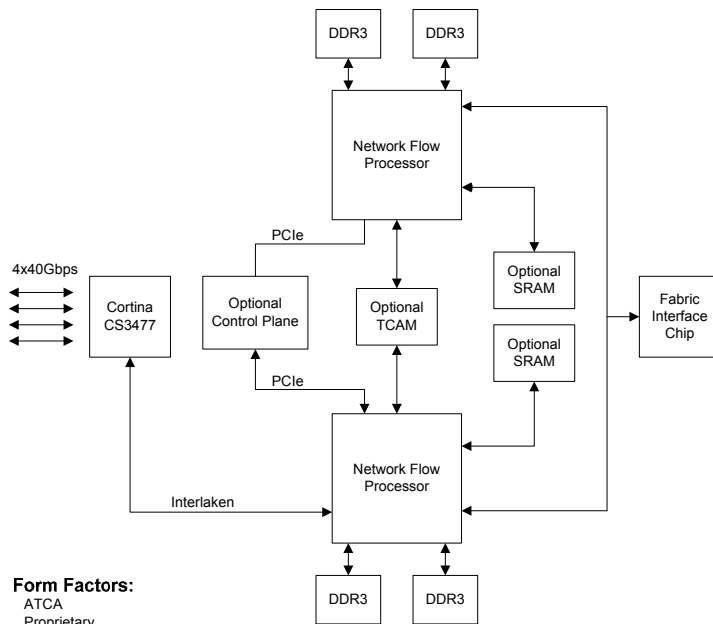
Also available from Netronome are supporting NFP Software Development Tools and an NFP-3200 Customer Development Platform.

Additional Integrated Hardware Features:

Internal hardware structures for function acceleration, ring support and general-purpose utilization maximize software application options for efficiency and performance:

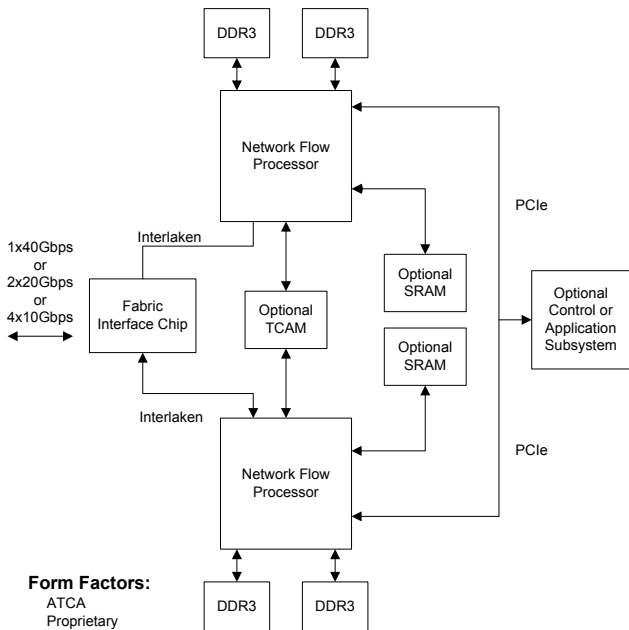
- Hardware hash unit (48-, 64-, and 128-bit)
- 16 KB scratchpad memory
- Serial UART port for debug
- 12 GPIO pins

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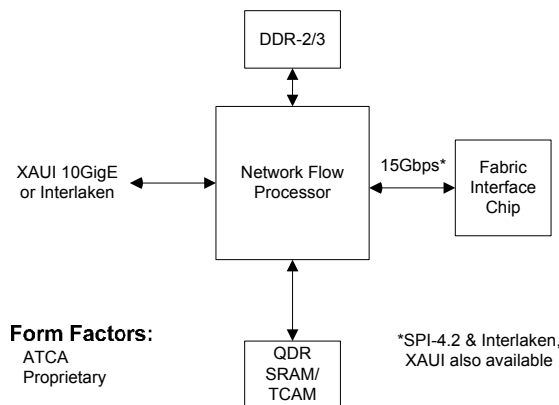
Form Factors:
ATCA
Proprietary

40Gbps Programmable Line Card



Form Factors:
ATCA
Proprietary

40Gbps Programmable Service Blade



Form Factors:
ATCA
Proprietary

*SPI-4.2 & Interlaken,
XAUI also available

Intelligent 10G Full-duplex Line Card

NFP-3200 Upgrades over the IXP288XX

16 microengines (v2.5) upgraded to 40 microengines (v2.7)

The additional 24 microengines more than doubles the processing capability while remaining code-compatible with the IXP28XX NPU. Version 2.7 of the microengine enables 16k of programmable control store by pairing NFP microengines, and adds both ECC protection on the control stores and parity on the registers and local memory.

RDRAM replaced with DDR3 DRAM

The DDR3 memory interface provides customers with a means to increase their overall memory capability (2x performance and 4x the capacity), while significantly reducing the system cost by a factor of 10.

PCI Upgraded to PCIe 2.0 (eight lanes)

The PCIe interface enables customers to use the NFP-3200 product family in both control plane and data plane applications.

Four QDR SRAM channels are replaced with two physical QDR SRAM channels and two virtual QDR channels

This change offers customers a higher performance, lower-cost approach to attaining SRAM bandwidth, in terms of queuing operations (>5x performance increase). For applications requiring only two QDR SRAM channels, no external parts are required.

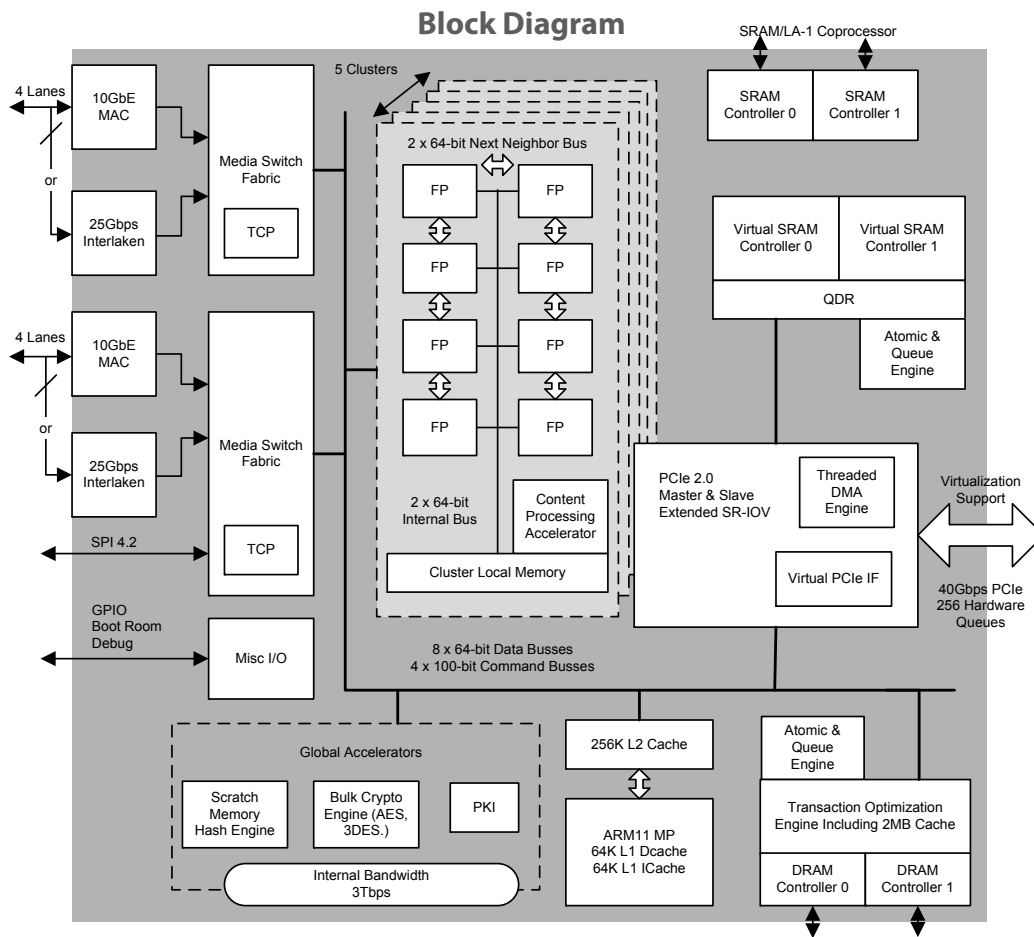
The integrated host Intel Xscale® Core is replaced by an ARM11 Core

The ARM11 Core has 256 kB of L2 cache that increases the performance capabilities of the core.

A second Media Switch Fabric (MSF) Interface has been added along with additional new features

The second MSF interface supports NFP usage in full-duplex configurations. The new features provide customers with a richer set of interface alternatives including XAUI (1x10 Gbps or 4x1 Gbps) or 4x6.25 Gbps lanes of Interlaken.

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Ordering Information

SiNFP-3240-0-A2-AM10	1.4 GHz, 40 Fps, highest performance NFP SKU
SiNFP-3240-0-A2-BM10	1.3 GHz, 40 Fps, highest performance NFP SKU
SiNFP-3240-0-A2-CM10	1.2 GHz, 40 Fps, highest performance NFP SKU
SiNFP-3240-0-A2-DM10	1.0 GHz, 40 Fps, highest performance NFP SKU
SiNFP-3240-8-A2-AM10	1.4 GHz, 40 Fps, with crypto
SiNFP-3240-8-A2-BM10	1.3 GHz, 40 Fps, with crypto
SiNFP-3240-8-A2-CM10	1.2 GHz, 40 Fps, with crypto
SiNFP-3240-8-A2-DM10	1.0 GHz, 40 Fps, with crypto
SiNFP-3224-0-A2-AM10	1.4 GHz, 24 Fps, no crypto value SKU
SiNFP-3224-0-A2-BM10	1.3 GHz, 24 Fps, no crypto value SKU
SiNFP-3224-0-A2-CM10	1.2 GHz, 24 Fps, no crypto value SKU
SiNFP-3224-0-A2-DM10	1.0 GHz, 24 Fps, no crypto value SKU
SiNFP-3224-8-A2-AM10	1.4 GHz, 24 Fps, with crypto
SiNFP-3224-8-A2-BM10	1.3 GHz, 24 Fps, with crypto
SiNFP-3224-8-A2-CM10	1.2 GHz, 24 Fps, with crypto
SiNFP-3224-8-A2-DM10	1.0 GHz, 24 Fps, with crypto
SiNFP-3216-8-A2-AM10	1.4 GHz, 16 Fps, with crypto
SiNFP-3216-8-A2-BM10	1.3 GHz, 16 Fps, with crypto
SiNFP-3216-8-A2-CM10	1.2 GHz, 16 Fps, with crypto
SiNFP-3216-8-A2-DM10	1.0 GHz, 16 Fps, with crypto