Tsi106™:
Power PC™ Host Bridge
Product Feature Sheet

Features:

Processor Interface

- Supports the following Motorola processors: MPC603e, MPC740, MPC745, MPC750, MPC755, MPC7400, and MPC7410
- Supports the following IBM processors: PowerPC 603e, PowerPC 740, and PowerPC 750
- Processor bus frequency up to 83 MHz
- 64-bit data bus and 32-bit address bus
- Supports either an external L2 cache or a secondary processor
- Full memory coherency supported

Memory Interface

- Supports DRAM (page mode, EDO), and SDRAM
- 64-bit data bus that operates up to 66 MHz
- Supports 1 to 8 banks built of x1, x4, x8, x9, x16 or x18 DRAM chips
- 1 GB of RAM space, 16 MB of ROM space
- Supports writing to Flash EPROMs
- Supports parity or error-correcting code (ECC)

PCI Interface

- Compliant with PCI Specification, (Revision 2.1)
- Supports up to 33 MHz operation
- Read and write buffers to improve PCI performance
- Supports concurrent transactions on processor and PCI buses
- 3.3 V/5 V compatible

Packaging

- 304-pin, ceramic ball grid array (CBGA)
- Package outline 21 mm x 25 mm, 1.27 pitch

Device Overview

Tsi106™ PowerPC™ Host Bridge provides proven system interconnect between PowerPC host processors and the PCI bus. PCI support allows system designers to develop systems quickly using peripherals already designed for PCI and the other standard interfaces available in the personal computer industry.

The Tsi106™ integrates secondary cache control and a high-performance memory controller that supports DRAM, SDRAM, ROM, and Flash ROM. The Tsi106™ uses an advanced, 3.3 V CMOS process technology and is fully compatible with TTL devices.

Multiprocessor and L2 Cache Support

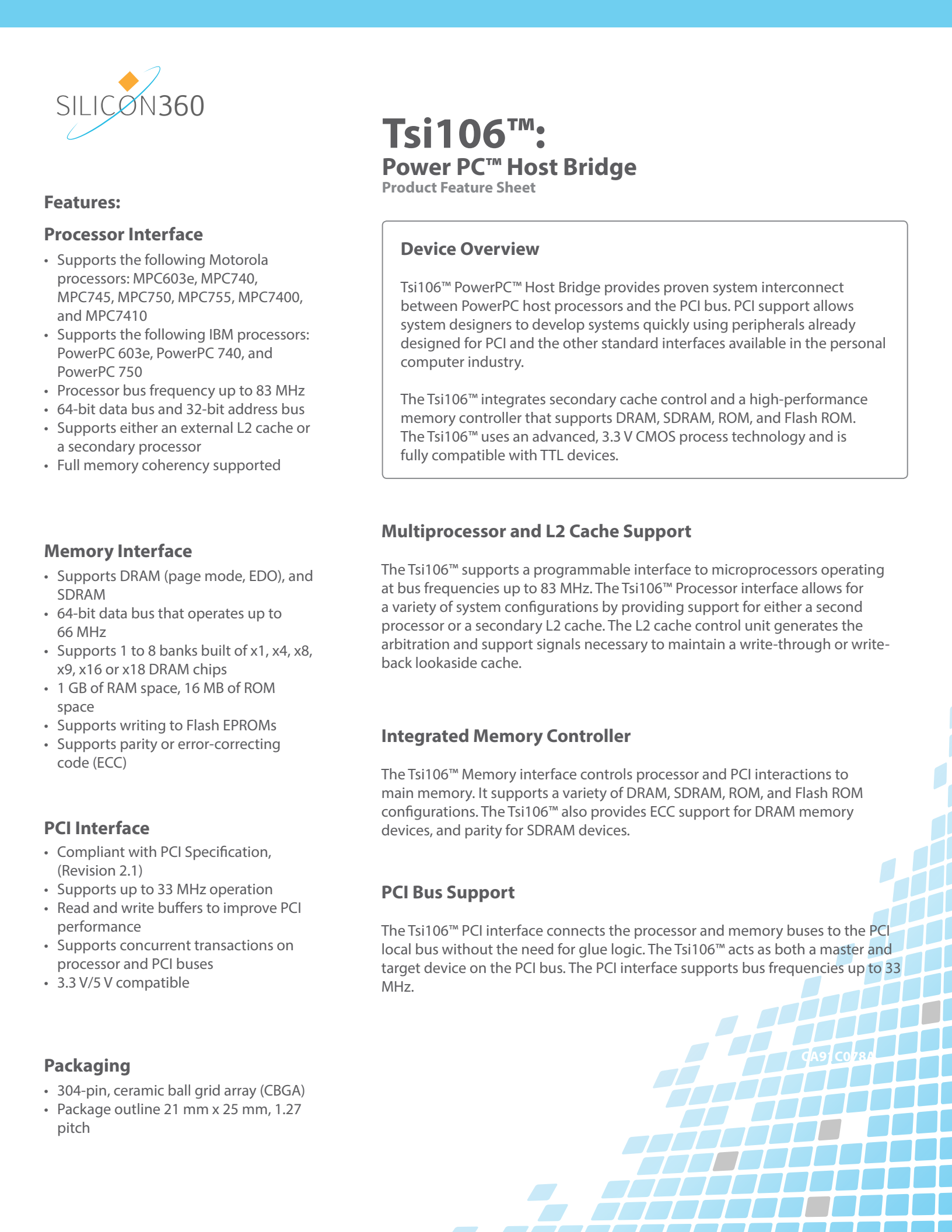
The Tsi106™ supports a programmable interface to microprocessors operating at bus frequencies up to 83 MHz. The Tsi106™ Processor interface allows for a variety of system configurations by providing support for either a second processor or a secondary L2 cache. The L2 cache control unit generates the arbitration and support signals necessary to maintain a write-through or write-back lookaside cache.

Integrated Memory Controller

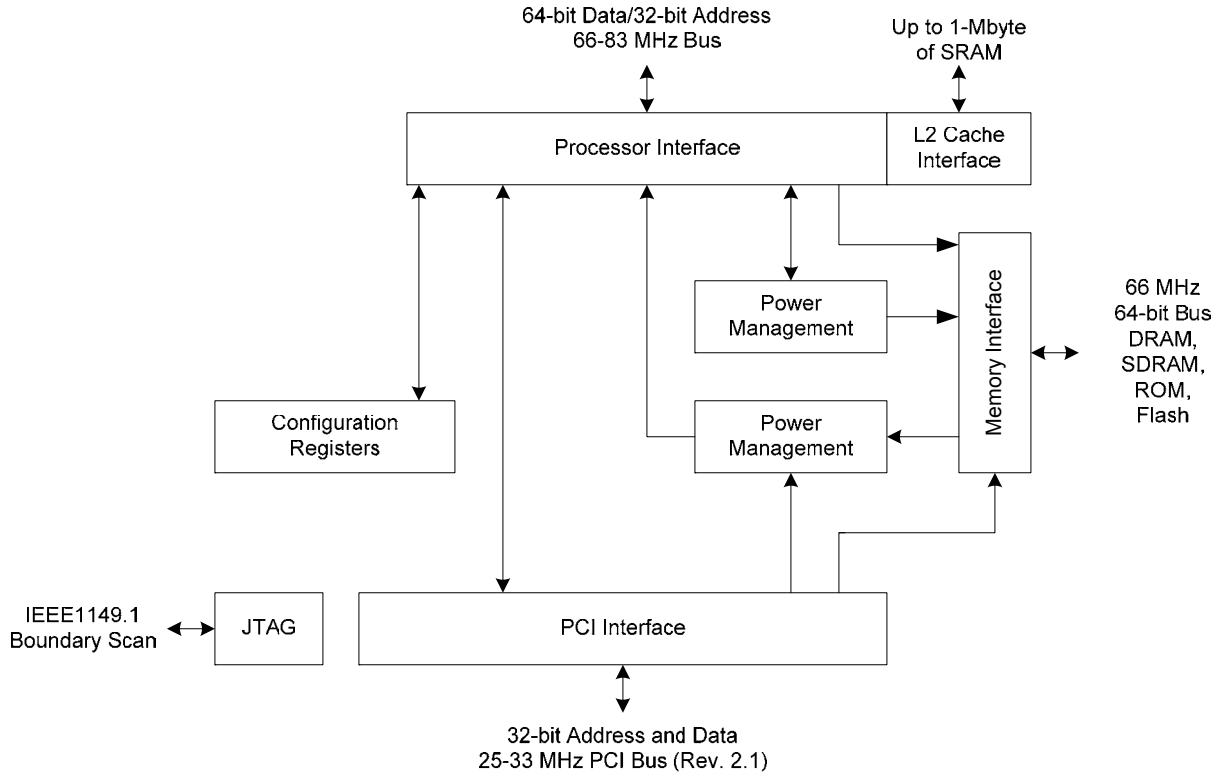
The Tsi106™ Memory interface controls processor and PCI interactions to main memory. It supports a variety of DRAM, SDRAM, ROM, and Flash ROM configurations. The Tsi106™ also provides ECC support for DRAM memory devices, and parity for SDRAM devices.

PCI Bus Support

The Tsi106™ PCI interface connects the processor and memory buses to the PCI local bus without the need for glue logic. The Tsi106™ acts as both a master and target device on the PCI bus. The PCI interface supports bus frequencies up to 33 MHz.



Tsi106 Block Diagram



Secondary Cache Control

- 256 KB, 512 KB, 1 MB sizes
- Direct-mapped
- Provides support for either asynchronous SRAM, burst SRAM, or pipelined burst SRAM
- Supports external lookaside L2 cache controller

Other Features

- IEEE 1149.1-compliant, JTAG boundary-scan interface
- Available in commercial (0 to 105 °C junction temperature) and industrial (-40 to 105 °C junction temperature) temperature ranges

Power Management

The Tsi106 provides hardware support for four levels of power reduction: nap, doze, sleep, and suspend. The Tsi106™ design is fully static, allowing internal logic states to be preserved during all power saving modes.

Part Number Information

Current Part Number	Obsolete Motorola Part Number
Tsi106G-66JB	MPC106ARX66CG
Tsi106G-66JBTR	MPC106ARX66CGR2
Tsi106G-66KB	MPC106ARX66TG
Tsi106G-83JB	MPC106ARX83DG
Tsi106G-83KB	MPC106ARX83TG