TDA9937:
Dual 10-bit DAC, Up to 750 Msps; 4x and 8x Interpolating
Product Feature Sheet

Features
- Dual 10-bit resolution
- IMD3: 74 dBc; f_s = 737.28 Msps; f_o = 140 MHz
- 750 Msps maximum update rate
- ACPR: 64 dBc; 2-carrier WCDMA; f_s = 737.28 Msps; f_o = 153.6 MHz
- Selectable 4x or 8x interpolation filters
- Typical 1.2 W power dissipation at 4x interpolation, PLL off and 740 Msps
- Input data rate up to 185 Msps
- Power-down and Sleep modes
- Very low noise cap-free integrated PLL
- Differential scalable output current from 1.6 mA to 22 mA
- 32-bit programmable NCO frequency
- On-chip 1.29 V reference
- Dual port or Interleaved data modes
- External analog offset control (10-bit auxiliary DACs)
- 1.8 V and 3.3 V power supplies
- Internal digital offset control
- LVDS compatible clock
- Inverse x / (sin x) function
- Two's complement or binary offset data format
- Fully compatible SPI port
- 1.8 V/3.3 V CMOS input data buffers
- Industrial temperature range from -40 °C to +85 °C

Typical Applications
- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

Device Overview

The TDA9937 is a high-speed 10-bit dual channel Digital-to-Analog Converter (DAC) with selectable 4x or 8x interpolating filters optimized for multi-carrier wireless transmitters.

Thanks to its digital on-chip modulation, the DAC1005D750 allows the complex I and Q inputs to be converted from BaseBand (BB) to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register.

Two modes of operation are available: separate data ports or a single interleaved high-speed data port. In the Interleaved mode, the input data stream is demultiplexed into its original I and Q data and then latched.

A 4x and 8x clock multiplier enables the DAC1005D750 to provide the appropriate internal clocks from the internal PLL. The internal PLL can be bypassed enabling the use of an external high frequency clock. The voltage regulator enables adjustment of the output full-scale current.

Absolute Maximum Ratings:

Input/Output Supply Voltage (3.3 V)	-0.5 V to +4.6 V
Analog Supply Voltage (3.3 V)	-0.5 V to +4.6 V
Analog Supply Voltage (1.8 V)	-0.5 V to +3.0 V
Digital Supply Voltage (1.8 V)	-0.5 V to +3.0 V
Input Voltage (pins CLKP, CLKN, VIRES and GAPOUT referenced to AGND)	-0.5 V to +3.0 V
Input Voltage (pins I9 to I0, Q9 to Q0, SDO, SDIO, SCLK, SCS_N and RESET_N referenced to GNDIO)	-0.5 V to +4.6 V
Output Voltage (pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP AND AUXBN referenced to AGND)	-0.5 V to +4.6 V
Output Voltage (pin SYNCP and SYNCN referenced to pin AGND)	-0.5 V to +3.0 V
Storage Temperature	-55 °C to +150 °C
Ambient Temperature	-40 °C to +85 °C
Junction Temperature	125 °C

Block Diagram