

# ICS852141:

## Low Skew, 1-to-5, Differential-to-HSTL Fanout Buffer

### Product Feature Sheet

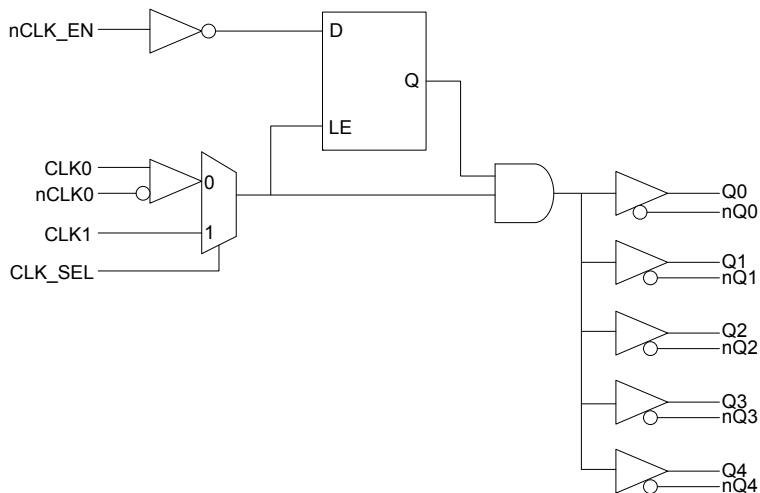
#### Features

- Five differential HSTL compatible outputs
- Selectable differential CLK0, nCLK0 or LVCMOS/LVTTL clock inputs
- CLK0, nCLK0 pair can accept the following differential input levels: LVDS, LVPECL, HSTL, HCSL
- CLK1 can accept the following input levels: LVCMOS or LVTTL
- Output frequency up to 700 MHz
- Translates any single ended input signal to HSTL levels with resistor bias on nCLK0 input
- Output skew: 40 ps (maximum)
- Part-to-part skew: 300 ps (maximum)
- 3.3 V core, 1.8 V output operating supply
- Available in Lead-Free (RoHS 6) package
- -40 °C to 85 °C ambient operating temperature

#### Device Overview

The ICS852141 is a low-skew, high-performance 1-to-5 differential-to-HSTL fanout buffer. The CLK0, nCLK0 pair can accept most standard input levels. The single-ended CLK1 input accepts LVCMOS or LVTTL input levels. Guaranteed output and part-to-part skew characteristics make the ICS852141 ideal for those clock distribution applications demanding well-defined performance and repeatability.

#### ICS852141 Block Diagram



#### ICS852141 Pin Assignment

Q0	1	20	V <sub>DD0</sub>
nQ0	2	19	nCLK_EN
Q1	3	18	V <sub>DD</sub>
nQ1	4	17	nc
Q2	5	16	CLK1
nQ2	6	15	CLK0
Q3	7	14	nCLK0
nQ3	8	13	nc
Q4	9	21	CLK_SEL
nQ4	10	11	GND

#### ICS852141 20-Lead TSSOP

6.5 mm x 4.4 mm x 0.92 mm package body

#### G Package Top View