SILICON360

ADC1207S080:

Single 12 Bits ADC, Up to 80 MHz with Direct/Ultra High IF Sampling

Product Feature Sheet

Features

- 12-bit resolution
- Differential input with 375 MHz bandwidth
- 90 dB SFDR; 71 dB S/N (fi = 225 MHz; fclk = 80 MHz; B = 5 MHz)
- 74 dB SFDR; 66.5 dB S/N (fi = 175 MHz; fclk = 80 MHz; B = Nyquist)
- High speed sampling rate up to 80 MHz
- Internal front-end buffer (input capacitance < 1 pF)
- Programmable acquisition output clock (complete conversion signal)
- Full-scale controllable from 1.5 V to 2 V (p-p); continuous scale
- Single 5 V power supply
- 3.3 V LVCMOS compatible digital outputs
- Binary or two's-complement LVCMOS outputs
- CMOS compatible static digital inputs
- Only 2 clock cycles latency
- Industrial temperature range from -40 °C to +85 °C
- HTQFP48 package

Typical Applications

- Radio transceivers
- Wireless infrastructure
- Cable modem
- Digital storage scope
- Fixed telecommunication,
- Optical networking
- Wireless Local Area Network (WLAN) infrastructure.
- General purpose applications

Device Overview

The ADC1207S080 is a 12-bit Analog-to-Digital Converter (ADC) optimized for direct Input Frequency (IF) sampling and supporting the most demanding use conditions in ultra high IF radio transceivers for cellular infrastructure and other applications such as wireless infrastructure, optical networking and fixed telecommunication. Due to its broadband input capabilities, the ADC1207S080 is ideal for single and multiple carriers data conversion.

Operating at a maximum sampling rate of 80 MHz, analog input signals are converted into 12-bit binary coded digital words. All static digital inputs are CMOS compatible. All output signals are Low-Voltage Complementary Metal-Oxide Semiconductor (LVCMOS) compatible. The ADC1207S080 offers the most flexible acquisition control system because of its programmable Complete Conversion Signal (CCS) that allows to adjust the delay of the acquisition clock.

The ADC1207S080 offers the lowest input capacitance (< 1 pF) and therefore the highest flexibility in front-end aliasing filter strategy because of its internal front-end buffer.

Absolute Maximum Ratings:

Analog Supply Voltage	-0.5 V to +7.0 V
Digital Supply Voltage	-0.5 V to +7.0 V
Output Supply Voltage	-0.5 V to +5.0 V
Supply Voltage Difference: V_{CCA} - V_{CCD}	-1.0 V to +1.0 V
Supply Voltage Difference: V_{CCD} - V_{CCO}	-1.0 V to +4.0 V
Supply Voltage Difference: V_{CCA} - V_{CCO}	-1.0 V to +4.0 V
Input Voltage on Pin IN	V_{CCA} + 1 V
Input Voltage on Pin INN	V_{CCA} + 1V
Input Voltage on Pin CLK	V_{CCD} + 1 V
Input Voltage on Pin CLKN	V_{CCD} + 1 V
Output Current	10 mA
Storage Temperature	-55 °C to +150 °C
Ambient Temperature	-40 °C to +85 °C
Junction Temperature	150 °C

Block Diagram